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ANN Based Voltage Flicker Mitigation with UPFC Using SRF Algorithm

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Abstract
Voltage flicker, a phenomenon of annoying light intensity fluctuation, caused by rapid change in industrial and domestic load such as arc furnace operating periodically has been a major concern for supplying utilities and customers in the vicinity. The arc furnace current is of quasi-periodic with a frequency of about 10 Hz causing perceptible flicker. The FACTS devices like SVC's, STATCOM, UPFC and Custom Power devices like DSTATCOM have been able to solve the voltage flicker problems by rapidly controlling the reactive power. But, control of active power along with reactive power control helps to mitigate the voltage flicker problem more effectively. In this paper, voltage flicker mitigation with UPFC is analyzed using the MATLAB software. The proposed ANN based control algorithm controls the flicker effectively. The control algorithm is based on synchronous reference frame (SRF) method. This algorithm controls both active power and reactive power simultaneously. When the series converter of UPFC compensates voltage flicker, the shunt converter replenishes dc link energy storage. A self charging circuit is used to maintain dc link voltage. The dynamic operation is investigated using this algorithm.

Keywords: Voltage flicker, Synchronous Reference Frame algorithm, Artificial Neural Network, Unified Power Flow Controller.

1. Introduction

Power quality is the term used to describe how closely the electrical power delivered to customers conforms to the appropriate standards in operating their end-use equipment correctly. Thus, it is essentially a customer-focused measure although greatly affected by the operation of the distribution and transmission network. There are number of ways in which the electric supply can deviate from the specified measures. These range from transients and short duration variations to long-term waveform distortions. Sustained complete interruptions of supply are generally considered as an issue of network reliability rather than power quality. The growing importance of power quality is due to the increasing use of sensitive load equipments including computer-based controllers and power electronic converters [Working group of UIE, 1992]. Besides, the customers are well aware of the commercial consequences of disturbances originating on the power system.Voltage flicker is caused by loads that exhibit continuous, rapid variations in load current. Arc furnaces are the most common cause for voltage flicker [D. O'Kelly et al., 1992]. Electric arc furnace, the main generator of voltage flicker, behaves in the form of a constant reactance and a variable resistance. The transformer-reactance system is modeled as a lumped reactance, a furnace reactance (included connection cables and busses) and a variable resistance [M. Zouiti et al., 1998] which models the arc. Voltage flicker appears as a modulation of the 60Hz waveform, similar to an amplitude modulated radio signal. It's expressed as a percentage by dividing the RMS value of

the modulating wave by the RMS value of the fundamental wave. In lighting systems, voltage flicker values as low as 0.5% can be perceptible to the human eye. Flicker values of 3% are downright irritating. Flicker is illustrated in figure 1 which shows the periodic variation in voltage peaks. The voltage flicker phenomenon is produced by voltage fluctuation in a power system due to time in-variant loads. Voltage flicker affect motor starting results in temperature rise and motor overloading. It affects control systems; reduce the lifetime as well as degradation of performance of the electronic, incandescent, and fluorescent and CRT devices. It has been also observed that the voltage fluctuations led to small speed variations of electrical motor results in variations in final quality of products [M. Bollen et al., 2006]. The IEC 61000-3-3 [1994] provides and explains voltage flicker limits for the equipments connected to LV systems. Hence voltage flicker mitigation becomes very important. The voltage variations and mitigation studies for equipments like arc furnaces, electric welders, motors, generators and wind turbines, can be found in [M.M. Morcos et al., 2002]. Voltage flicker mitigation depends on reactive power control [M. Zouiti et al., 1998]

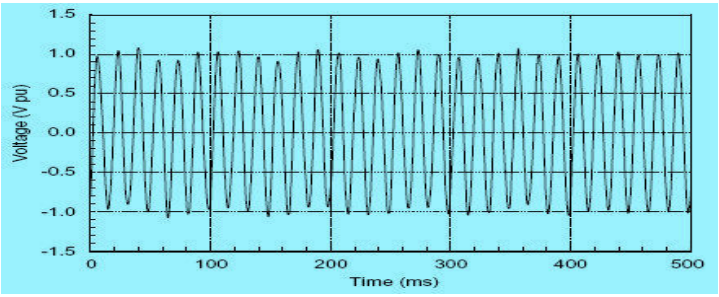

Figure 1. Illustration of voltage flicker

FACTS devices have been gradually introduced for voltage flicker compensation. The most used device for compensation of arc furnaces is the Static Var Compensator (SVC) [Poumarède C et al., 1997]. A major advantage is that reactive power supplied by the SVC increases the steel production. However, due to the operation with switching at fundamental frequency, conventional SVC have disadvantages such as relatively long response time and the possibility to only compensate for the fundamental frequency reactive current of the load. This limits the possibilities to reduce flicker with an SVC. Further, an SVC also introduces harmonics, and therefore it has to be combined with a passive filter bank. Flicker mitigation devices can also be connected in series with the arc furnace [P. Samuelsson et al., 1995]. The major advantages of series compensators over the parallel active compensators are that it can maintain the output voltage waveform to be sinusoidal and balance the three phase voltages. However, the series compensator is less popular in the industrial applications due to the inherent drawbacks of series circuits, namely it must handle high load currents, which increases their current rating compared with the parallel active power filters. As a result, the hybrid compensators are suitable for high-power applications. Unified Power Flow Controller (UPFC) has been widely used to mitigate voltage flicker. The UPFC with series active compensation capability opposed to variations of the arc resistance and suppress voltage flicker at the source [A. Elnady et al., 2002].

The control strategy adopted to mitigate flicker plays a key role for effective mitigation. Different control algorithms for flicker mitigation are presented in [J. Dolezal et al., 2000]. SVC devices achieved an acceptable level of mitigation, but because of their complicated control algorithms, they have problems such as injecting a large amount of current harmonics to the system and causing spikes in voltage waveforms. A new technique based on a novel control algorithm, which extracts the voltage disturbance to suppress the voltage flicker, is presented in [R. Mienski et al., 2004, Amit K et al., 2004]. The technique is to use STATCOM for voltage flicker compensation to overcome the aforementioned problems related to other techniques. The concept of instantaneous reactive power components is used in the controlling system. The UPFC with series active compensation capability opposed to variations of the arc resistance and suppress voltage flicker at the source. The design and control strategy of the UPFC based on the instantaneous power calculation are detailed in [Sedraoui.K et al., 2006]. SRM algorithm is commonly used for harmonic filtering. This algorithm relies on park transformations to transform the three phase system from a stationary reference frame into synchronously rotating direct, quadrature and zero sequence components. These can easily be analyzed since the fundamental frequency component is transformed into DC quantities. The active and reactive components of the system are represented by the direct and quadrature components respectively. This algorithm can be used for

voltage flicker mitigation. The computation is instantaneous but incurs time delays in filtering the DC quantities. The presence of these integral loops incorporates time delays, which depend on the frequency response of special feed forward and feedback integrators. In order to overcome these drawbacks, ANN based control algorithm for voltage flicker mitigation is proposed in this paper. Feed forward back propagation neural network architecture is used. The SRF algorithm is used for generating training data. Back propagation algorithm is used for training the ANN. Furthermore, a modified self-charging technique is used for maintaining dc bus voltage, which does not use PI controller.

2. Control structure of UPFC

From the conceptual viewpoint, the UPFC is a generalized synchronous voltage source (SVS), represented at the fundamental frequency by voltage phasor V_{pq} with controllable magnitude ($0 \leq V_{pq} \leq V_{pqmax}$) and angle ρ ($0 \leq \rho \leq 2\pi$), in series with the transmission line, as illustrated for the usual elementary two-machine system in figure 2. In this functionally unrestricted operation, which clearly includes voltage and angle regulation, the SVS generally exchanges both reactive and real power with the transmission system. Since an SVS is able to generate only the reactive power exchanged, the real power must be supplied to it, or absorbed from it, by a suitable power supply or sink. In UPFC arrangement the real power exchanged is provided by one of the end buses (e.g., the sending-end bus), as indicated in Figure 2.

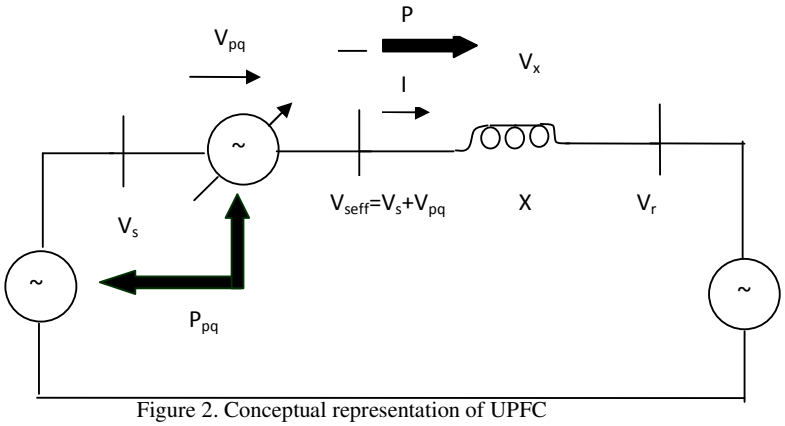

Figure 2. Conceptual representation of UPFC

The basic diagram of UPFC is shown in figure 3. In the presently used practical implementation, the UPFC consists of two voltage sourced converters, as illustrated in figure 3. These back-to-back converters are operated from a common dc link provided by a dc storage capacitor. Thus UPFC has two-voltage source converters connected back to back through a common dc bus. The converter-1 is called shunt converter and converter-2 is called series converter.

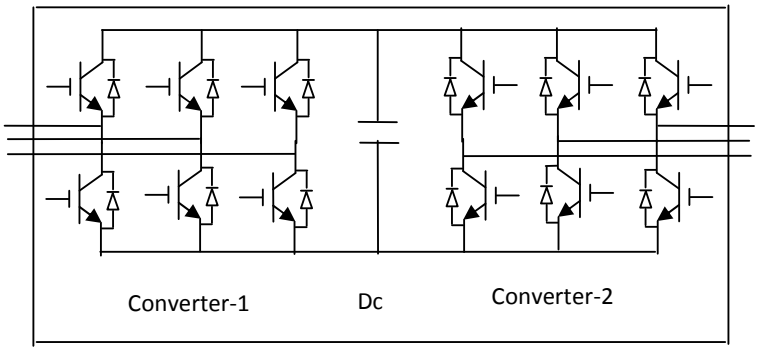

Figure 3. Two converter model of UPFC

The arrangement functions as an ideal ac to ac power converter in which real power can freely flow in either direction between the ac terminals of the two converters, and each converter can independently generate (or absorb) reactive power at its own ac output terminal. Converter-2 provides the main function the UPFC by injecting a voltage V_{pq} with controllable magnitude $|V_{pq}|$ and phase angle ρ in series with the line via an insertion transformer. This injected voltage acts essentially as a synchronous ac voltage source. The transmission line current flows through this voltage source resulting in reactive and real power exchange between it and its ac system. The reactive power exchanged at the ac terminal (ie. at the terminal of series injection transformer) is generated internally by the converter. The real power exchanged at the ac terminal is converted into dc power, which appears at the dc link as a positive or negative real power demand.

The basic function of converter-1 is to supply or absorb the real power demanded by converter-2 at the common dc link to support the real power exchange resulting from the series voltage injection. Converter-1 can also generate or absorb controllable reactive power if desired, and thereby provide independent shunt reactive compensation for the line. The superior operating characteristic of UPFC are due to its unique ability to inject an AC compensating voltage vector with arbitrary magnitude and angle in series with the line up on command, subject only to equipment rating limit with suitable electronic control. The UPFC can cause the series injected voltage vector to vary rapidly and continuously in magnitude and/or angle as desired. Thus it is not only able to establish an operating point within a wide range of possible P,Q conditions on the line , but also has the inherent capability to transition rapidly from one such achievable operating point to any other.

3. Modified SRF algorithm for flicker mitigation

SRM algorithm is commonly used for harmonic filtering. This algorithm relies on park transformations to transform the three phase system from a stationary reference frame into synchronously rotating direct, quadrature and zero sequence components. These can easily be analyzed since the fundamental frequency component is transformed into DC quantities. The active and reactive components of the system are represented by the direct and quadrature components respectively. This algorithm can be modified to suit voltage flicker mitigation.

The phase voltages (V_a, V_b, V_c) at PCC are sensed and given as input (V_{abc}) to SRF controller. The controller performs 3-ϕ to 2- ϕ conversion using equation (1) and the resultant variables V_d and V_q are expected to be pure dc if there is no flicker in input voltage. The oscillating components in V_d and V_q corresponds to voltage flicker component which is to be supplied by the series converter of UPFC. In order to separate the oscillating components of V_d and V_q, dc components are separated using low pass filter (LPF) and the same is subtracted from V_d and V_q to get oscillating components V_d* and V_q*.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \sqrt{\frac{3}{2}} & -\sqrt{\frac{3}{2}} \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{1}$$

This oscillating components V_d* and V_q* are converted from 2-ϕ to 3-ϕ using equation (2). The resulting signal V_{abc}* (V_a*, V_b*, V_c*) is given to PWM controller for producing firing pulses for series converter of UPFC.

$$\begin{bmatrix} v_a^* \\ v_b^* \\ v_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \sqrt{\frac{3}{2}} & -\sqrt{\frac{3}{2}} \end{bmatrix}^T \cdot \begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} \tag{2}$$

4. ANN based controller for flicker mitigation

The computations in SRF algorithm are instantaneous but incur time delays in filtering the DC quantities. The presence of these integral loops incorporates time delays, which depend on the

frequency response of special feed forward and feedback integrators. In order to overcome these drawbacks, ANN based control algorithm for voltage flicker mitigation is proposed in this paper. Artificial Neural Networks are predictive models loosely based on the action of biological neurons. The neural network used for flicker mitigation is full-connected, three layer, feed-forward, back propogation network. The input layer has three neurons. The three phase voltages (V_a, V_b, V_c) at PCC are sensed and given as input to ANN. Vector of predictor variable values is presented to the input layer. The input layer standardizes these values so that the range of each variable is -1 to 1. The input layer distributes the values to each of the neurons in the hidden layer. There is only one hidden layer with three neurons. Arriving at a neuron in the hidden layer, the value from each input neuron is multiplied by a weight, and the resulting weighted values are added together producing a combined value. The weighted sum is fed into a transfer function, σ, which outputs a value. The outputs from the hidden layer are distributed to the output layer. Arriving at a neuron in the output layer, the value from each hidden layer neuron is multiplied by a weight, and the resulting weighted values are added together producing a combined value. The weighted sum is fed into a transfer function, σ, which outputs a value. These values are the outputs of the network. There are three neurons in the output layer which gives the reference voltages (V_a*, V_b*, V_c*) to PWM controller which in turn produces firing pulses for UPFC.

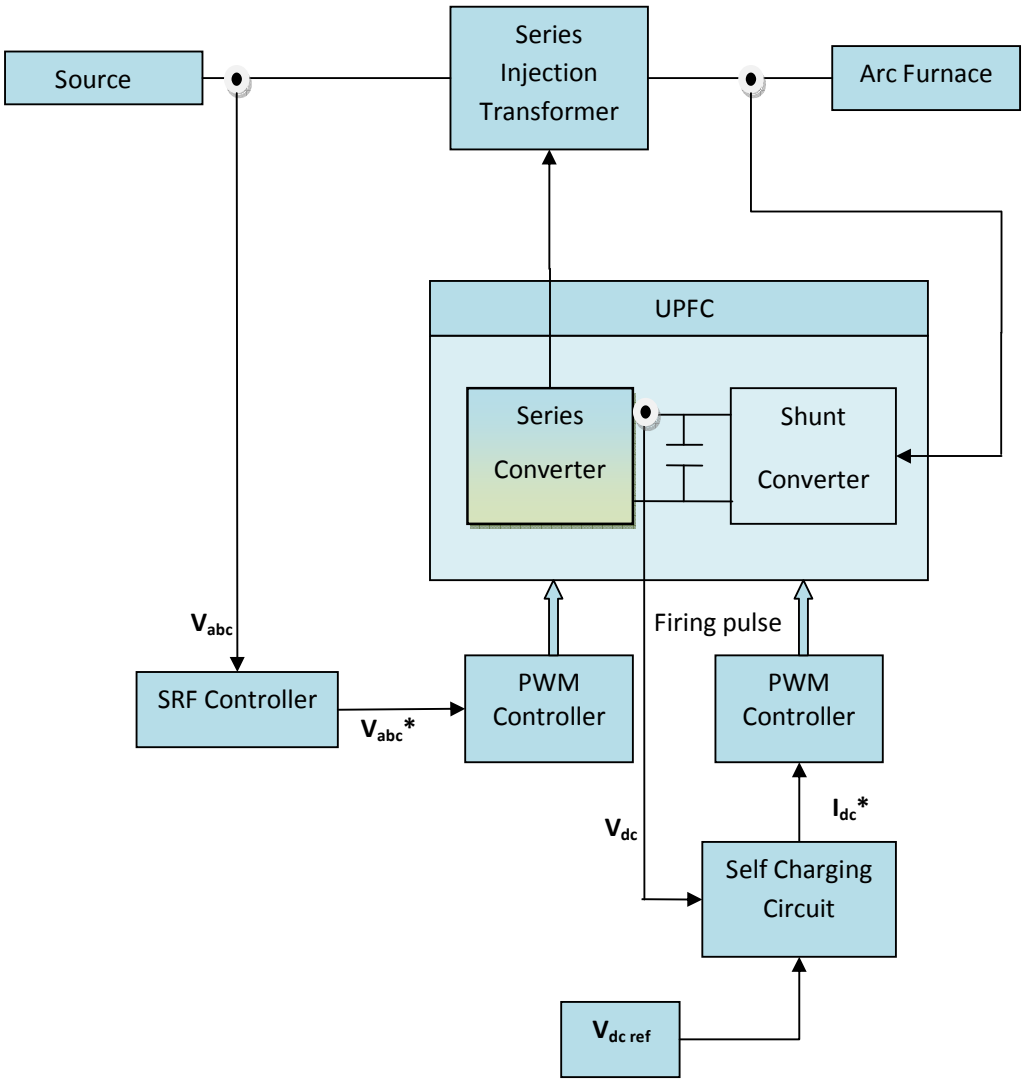

Figure 4. UPFC for flicker mitigation

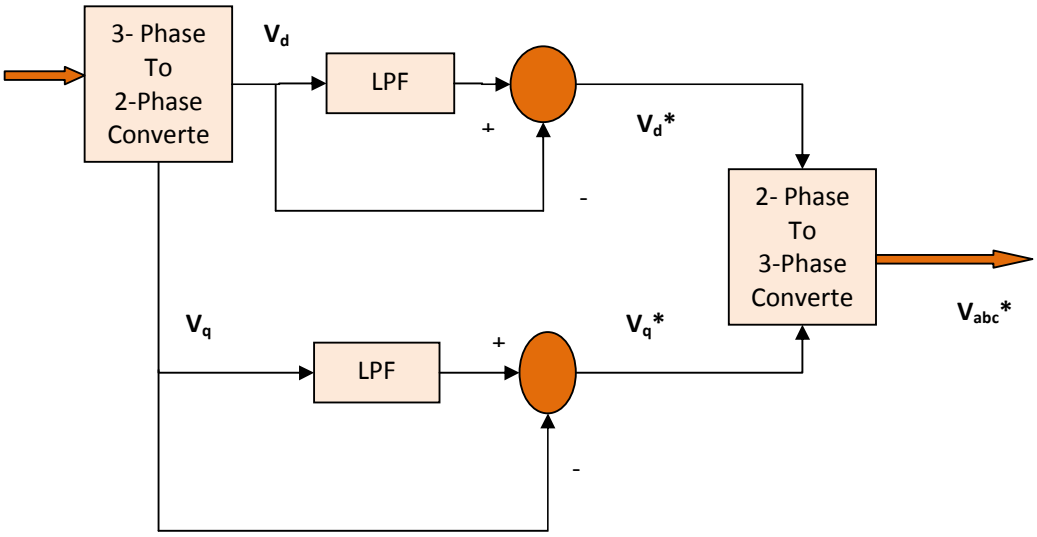

Figure 5. Modified SRF controller for flicker mitigation

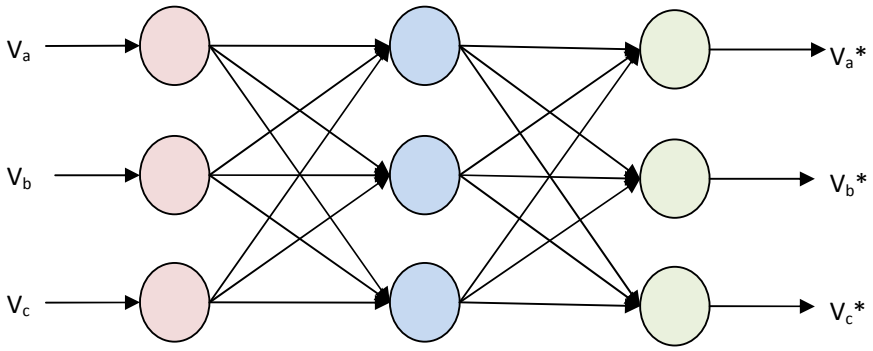

Figure 6 ANN based controller for flicker mitigation

5. Training of ANN

The goal of the training process is to find the set of weight values that will cause the output from the neural network to match the actual target values as closely as possible. Using flicker generator in MATLAB, flicker of various magnitude are generated and the corresponding reference signals are produced using SRF controller. These data are used for training the ANN. For fast convergence, back propagation training algorithm is used.

Given a set of randomly selected starting weight values, conjugate gradient algorithm is used to optimize the weight values. Most training algorithms follow this cycle to refine the weight values:

- Run a set of predictor variable values through the network using a tentative set of weights.
- Compute the difference between the predicted target value and the actual target value for this case.
- Average the error information over the entire set of training cases.
- Propagate the error backward through the network and compute the gradient (vector of derivatives) of the change in error with respect to changes in weight values.
- Make adjustments to the weights to reduce the error. Each cycle is called an epoch.

Because the error information is propagated backward through the network, this type of training method is called backward propagation.

6. Self charging circuit for maintaining dc bus voltage

To regulate the dc link capacitor voltage at the desired level, real power has to be drawn by the shunt converter of UPFC from the supply side to charge the capacitor. The configuration of three-phase self charging current is shown in Figure 7. The simple control algorithm is developed which does not use PI controller. To regulate the dc capacitor voltage at the desired level, an additional real power has to be drawn by the adaptive shunt active filter from the supply side to charge the two capacitors. The energy 'E' stored in each capacitor can be reprinted as

$$E = \frac{1}{2} C V_{dc}^{\ 2} \tag{3}$$

Where 'C' is the value of each capacitor and V_{dc} is the voltage of each capacitor. If the desired level of voltage across each capacitor is $V_{dc(ref)}$, the energy for capacitor is

$$E' = \frac{1}{2} C V_{dc(ref)}^{\ 2} \tag{4}$$

The difference between E¹ and E represents the additional energy required by capacitor to reach the desired voltage level. Thus

$$\Delta E = E^{|} - E = \frac{1}{2} C\left\{V_{dc(ref)}^{\ 2} - V_{dc}^{\ 2}\right\}. \tag{5}$$

On the other hand the charging energy E_{ac} delivered by the three phase supply side to the inventor of each capacitor will be

$$E_{ac} = 3pt$$
$$= 3(V_{rms} I_{dc(rms)} \cos\Phi)t. \tag{6}$$

p - Additional real power required; V_{rms} – RMS value of the instantaneous supply voltage

$I_{de(rms)}$ - RMS value of the instantaneous charging current; t – Charging time.

ϕ – Phase deference between the supply voltage and charging current

Here't' can be defined as T/2 since the charging process only takes place for half a cycle for each capacitor, where 'T' is the period of supply frequency. By using Phase Lock Loop (PLL) the charging current is made in phase with the supply voltage. Thus, power factor $\cos\phi = 1$. Also the RMS value can be expressed in terms of maximum values. This result in

$$E_{ac} = 3\frac{V}{\sqrt{2}}\frac{I_{dc}}{\sqrt{2}}\frac{T}{2}. \tag{7}$$

$$E_{ac} = \frac{3VI_{dc}T}{4} \tag{8}$$

Neglecting the switching losses in the inverter and according to the energy conservation law the following equation holds

$$\Delta E = E_{ac}$$
$$\frac{1}{2} C\left\{V_{dc(ref)}^{\ 2} - V_{dc}^{\ 2}\right\} = \frac{3VI_{dc}T}{4} \tag{9}$$
$$I_{dc} = 2C\frac{\left\{\left[V_{dc}(ref)\right]^2 - \left[V_{dc}\right]^2\right\}}{3VT} \tag{10}$$

To regulate the dc link capacitor voltage at the desired level, an additional real power has to be drawn by the IDVR from the supply side to charge the two capacitors. The configuration of three-phase self charging current is shown in Figure 7. The PLL synchronizes itself with the supply voltage of phase 'a' and outputs three sine waves which are 120° out of phase from each other. Three phase i_{dc} is obtained by multiplying these sine waves with the current I_{dc} which is calculated by the control algorithm. Thus, the three phase injection currents can be calculated as

$$
\begin{aligned}
i_{inj,a} &= -I_{dc} \sin \omega t \\
i_{inj,b} &= -I_{dc} \sin(\omega t - 120) \\
i_{inj,c} &= -I_{dc} \sin(\omega t + 120)
\end{aligned} \tag{11}
$$

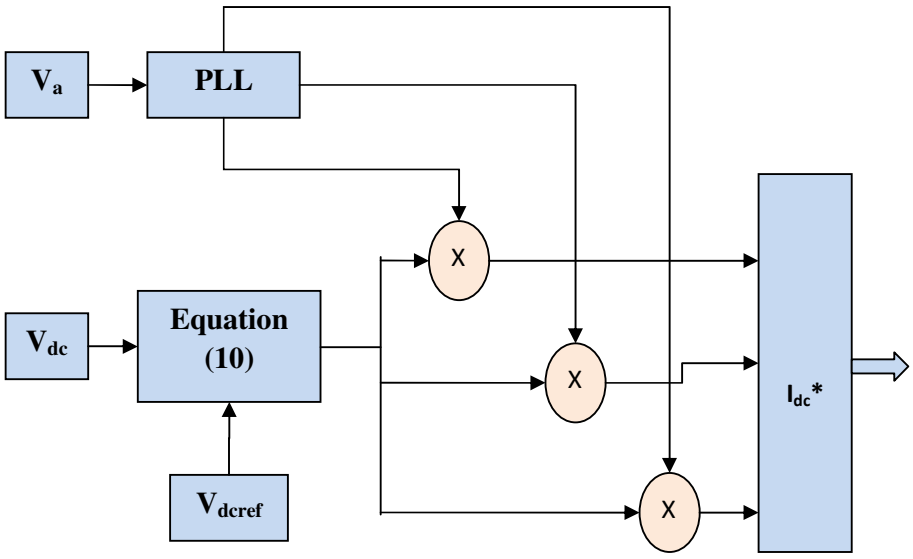

Figure 7. Three-phase self charging circuit

I_{dc}* denoted as output of self charging block in figure 4 is given as I_{dc}*= [$i_{inj,a}$, $i_{inj,b}$, $i_{inj,c}$] Where I_{dc} is given in equation (10). The minus sign indicates that the charging current i_{dc} flows into the UPFC. A PWM controller is used to control the switching of the shunt controller of UPFC.

7. Simulation studies

An arc furnace installation mostly consists of a large arc furnace used for melting scrap and a smaller ladle furnace used for the refining of the steel. The large arc furnace is creating the major part of the flicker problems. Usually the installation also contains some kind of compensating equipment to reduce the line disturbances caused by the furnace operation. The disturbances from the arc furnace are transferred to other users of electric energy via the Point of Common Connection, PCC. The voltage fluctuations causing flicker are then spread in the grid from the PCC with very low damping. The simplified representation of system with UPFC controller is shown in figure 4. Two transformers, T_1 and T_2, are included in the system and the simplified line diagram is shown in figure 8. T_1 (S_{N1} = 130 MVA, X_{T1}=11 %) is the transformer supplying power to the arc furnace bus. The nominal voltage on the bus between T_1 and T_2 is 31, 5 KV. T_2 (S_{N2} = 100 MVA, X_{T2}=8 %) is the transformer in arc furnace. The system has been simplified such that the model contains only the large arc furnace. At the top of Figure 8, the grid with a nominal short circuit power of 3600 MVA is shown. The arc furnace model is shown in figure 9. Simulation studies are done on the system with modified SRF controller and ANN based controller. The results obtained in both case are same and is shown in figure 11. The rms value of voltage at PCC before installation of UPFC is shown in figure 10.

Voltage flicker without UPFC is about 9% (ΔV/V). Flicker is mitigated and is 0.3% which is within IEEE threshold limits, when UPFC is connected at the PCC.

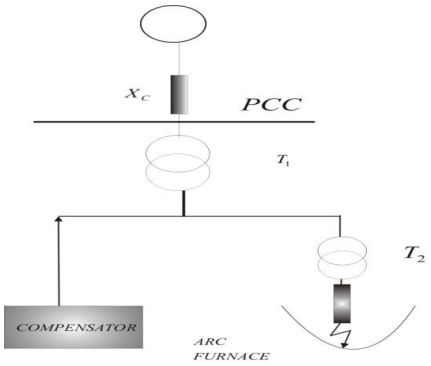

Figure 8. Typical arc furnace installations

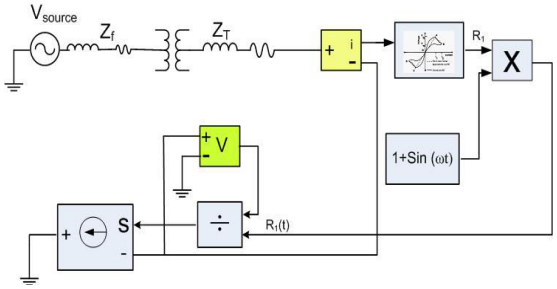

Figure 9**.** Model of arc furnace

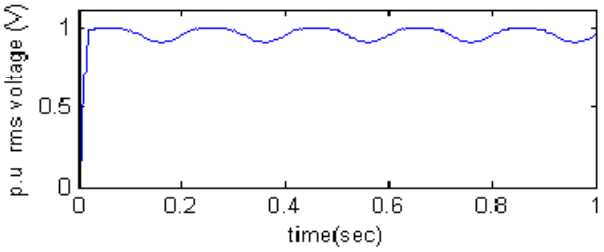

Figure 10**.** RMS value of voltage at PCC without UPFC

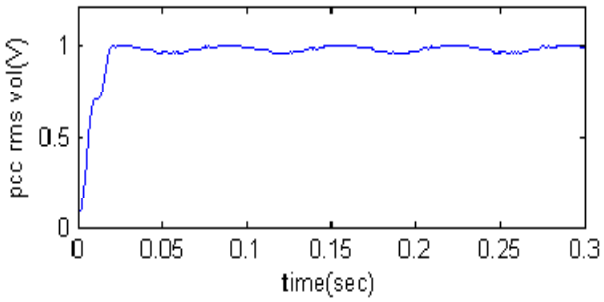

Figure 11. RMS value of voltage at PCC with UPFC

8. Conclusion

The basic control structure and functional control of UPFC is discussed. SRF controller used for harmonic filtering is modified to mitigate flicker using UPFC. The computations in SRF algorithm are instantaneous but incur time delays in filtering the DC quantities. The presence of these integral loops incorporates time delays, which depend on the frequency response of special feed forward and feedback integrators. In order to overcome these drawbacks, ANN based control algorithm for voltage flicker mitigation is proposed in this paper. Since the controls do not include any parameter which is dependent on network condition, the performance of such controller is robust with respect to network structure, fault location and system loading. The control structure is

decentralized and does not need any coordination with other compensating devices. The structure of proposed algorithm is easy to understand, easy to implement and attractive from a view-point of engineering. The model is simulated in MATLAB/SIMULINK platform and UPFC controller's performance is evaluated. Numerical simulation proved the effectiveness of the controller in compensating voltage flicker.

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