Development of a FPGA Based Real-Time Power Analysis and Control for Distributed Generation Interface

Alben Cardenas, *Member, IEEE*, Cristina Guzman, *Student Member, IEEE*, and Kodjo Agbossou, *Senior Member, IEEE*

***Abstract*—Energy coming from renewable sources has become very important nowadays, mainly because of their negligible contribution to greenhouse gas generation. A problem that then arises is how to integrate these new sources into a traditional power grid, in such a manner as to maximize the efficiency and reliability of this new distributed generation (DG) system. The hardware to do that is generally a voltage source inverter (VSI) that supplies a common load, as in single-phase residential and commercial applications. The optimizing process requires, of course, the usual power analysis. This paper presents the development and the experimental evaluation of a power control system for a single-phase grid-connected VSI including the power analysis using as processor for the control implementation a field-programmable gate array (FPGA) circuit. New hardware structures of adaptive linear neural networks (ADALINE) allow the implementation of power control algorithms and have also permitted the real-time analysis of the high-order harmonics without increasing the implementation area of the FPGA circuit. These features are ideal for novel DG power electronics interfaces that could be used not only for active power dispatch but also for harmonics and reactive power compensation. Simulation and experimental results of the proposed fixed and variable frequency schemes are included to confirm their validity.**

***Index Terms*—Artificial neural networks (ANNs), distributed power generation, harmonic analysis, programmable logic arrays, power measurement, total harmonic distortion.**

I. Introduction

NOWADAYS, the massive utilization of distributed energy resources (DER) based on renewable resources has become very important to mitigate problems related with greenhouse gas emissions and to improve the reliability and capability of actual and future power systems. The massive DER utilization is then promoted by governments and industry all around the world.

Developments on renewable energy systems and smart grid technologies are necessary to allow the integration of DER with the conventional centralized power systems. These technological advances will produce a high penetration of distributed generation (DG). New power electronics interfaces for grid-connected operation are also needed to take into account the local power control and additional functions including protections, islanding detection, power quality monitoring, and self diagnostics as the new tendencies toward smart integration modules (SIMs) [1]. This new approach must consider not only power dispatch, but also complementary functions such as the compensation of reactive power and harmonics and the embedded real-time monitoring of the power quality, the frequency, the voltage, and the active and reactive powers. Additionally detailed harmonics information will not be a choice but an important feature to be considered in the DG interfaces.

The harmonic content of electrical signals is commonly evaluated using the fast Fourier transform (FFT) [2] and recursive techniques such as the recursive least square (RLS) and the Kalman filter (KF) [3]–[6]. Artificial neural networks (ANNs) such as the adaptive linear neuron (ADALINE) [7]–[9] and the radial basis function neural network (RBFNN) [10] are also used. In recent literature works, the tracking of frequency and the estimation of a selected number of harmonics have been implemented using the multiresonant second-order generalized integrator frequency-locked loop (MSOGI-FLL) in [11] and using DFT implementation in [12]. The main drawbacks when applying the named methods are the high complexity for hardware implementation and the long computational time when software implementation is involved. Generally in literature, multiprocessor applications are used to meet real-time requirements when control and power quality monitoring are necessary, but the complexity and final cost will be consequently increased.

Lately, in many industrial sectors, the field-programmable gate array (FPGA) has become an interesting target for embedded applications, since its parallel structure reduces execution times [13]–[18]. This advantage is more evident when hardware implementations are considered.

Taking into account all important named characteristics needed to make possible the integration of DER in power systems, this paper presents the development and the experimental validation of a FPGA-based power analysis and control of a DG interface. The measurement and control algorithms use pure hardware architectures of ADALINE, as proposed in [19] and [20]. The proposed algorithms have been implemented in an FPGA circuit using Xilinx-System Generator and ISE Foundation for the Bitstream file generation and evaluated

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The authors are with the Hydrogen Research Institute and the Département de Génie électrique et Génie informatique, Université du Québec à Trois-Rivières, Trois-Rivières, QC, G9A 5H7 Canada (e-mail: alben.cardenas-gonzalez@uqtr.ca; kodjo.agbossou@uqtr.ca; cristina.guzman@uqtr.ca).

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experimentally by using grid-connected IGBT VSI. The evaluated application includes the following embedded functions: real-time tracking of the amplitude, the phase angle, and the frequency of the utility voltage, synchronization and power control of a single-phase grid-connected VSI, real-time estimation and monitoring of active and reactive powers, and real-time estimation and monitoring of voltage and current spectrums and total harmonic distortion. All mentioned functions are integrated into just one FPGA processor.

This paper is organized as follows. Section II presents some considerations of hardware and software implementations for real-time harmonics estimation. The development of ADALINE schemes for harmonic estimation using an FPGA is presented in Section III. The VSI synchronization and control, and the evaluation of the FPGA resources utilization are presented in Sections IV and V, respectively. Experimental results are provided in Section VI, and concluding remarks are given in Section VII.

II. Hardware and Software Implementations for Real-Time Harmonics Estimation

FFT-, RLS-, and KF-based methods for harmonics estimation are normally implemented using software applications in digital signal processors (DSPs) or personal computer (PC) targets. These kinds of applications exhibit long computational time and would be useful only when online power analysis is not required or a small number of harmonics are analyzed. Consequently, the long execution time of software implementations, for high-order harmonics estimation, results in a reduction of the sampling rate and of the estimation accuracy.

Learning algorithms based on ANNs such as the ADALINE are also employed for signal estimation and harmonics detection. The ADALINE technique has been used for envelope tracking detection [5], [21], [22], harmonics estimation of electrical signals [23]–[25], control applications [26], [27], and active filters [28], [29]. Recent work using ANNs implementation for harmonics detection, such as RBFNN [10], shows that this method produces more accurate results than ADALINE and FFT methods. However, the implementation cost is higher due to the increase in the use of multipliers when the number of samples of the analyzed signal and as well as the harmonic order of the estimation become higher.

Research publications indicate that most of the hardware FPGA implementations for harmonics estimation use direct or pipelined structures that offer very short execution times, which is ideal for signal processing applications such as in telecommunication systems. Direct implementation structures require a high use of arithmetic blocks (adders and multipliers), which are limited resources in FPGA systems. On the other hand, hardware FPGA implementations of ANNs and digital filters are more efficient than software implementations if the algorithm speed is the main objective.

An important fact in power systems applications is that the voltage and current signals, including their corresponding harmonics, have much lower frequencies than the one of the FPGA clock. In that case, direct or pipelined implementations for voltage and current estimation in power systems results in an unnecessary increase of the FPGA area utilization. This area increase is more important when high-order harmonics estimation is required. Hence, a compromise between execution time and implementation area must be realized in order to obtain the most efficient cost-speed relation.

III. Proposed FPGA Implementation of ADALINE

A periodic signal $y(t)$ with angular frequency ω may be calculated in

$$y(t) = A_0 + \sum_{n=1}^{\infty} [A_n \cos(n\omega t) + B_n \sin(n\omega t)] \quad (1)$$

by using its Fourier series representation, and it may be represented according to the ADALINE linear combiner equation [8], [9]

$$\hat{y}(k) = W_0(k) + W(k)^T \cdot X(k) \quad (2)$$

where $\hat{y}(k)$ represents the estimated signal which is calculated with the input pattern vector X containing the N harmonic components sine and cosine, the weight vector W which represents the Fourier coefficients, and W_0 which is the estimated average of the measured signal.

In this application, the Widrow–Hoff learning rule

$$W(k+1) = W(k) + \frac{\alpha}{N} \cdot e(k) \cdot X(k) \quad (3)$$

is employed to update the weight vector [8], [9], where α is a learning factor typically chosen between 0 and 2, and $e(k)$ is the estimation error calculated at the k instant using the measured and sampled signal $y(k)$ and its estimated value (2).

The proposed implementation of ADALINE is composed of a common block for the X vector generation function, and a modular block for each channel for sample and normalization, the W vector updating and the signal estimation functions. In order to calculate correctly the estimated signal and the estimation error within the sampling period (T_S), a common block has been created to allow the synchronized sampling of the input ports, the generation of the X vector and the W vector updating functions.

A. Generation of the Input Pattern Vector

The direct digital synthesis (DDS) technique [30], [31] is commonly employed to generate periodic signals using a discrete time phase generator and a phase-to-waveform converter. An FPGA implementation of a fixed-frequency DDS (FF-DDS) has been proposed in previous work [19]. A new structure which works at variable frequency (VF-DDS) is also proposed to generate the X vector [20]. The novelty of the proposed implementation structures of DDS (FF-DDS and VF-DDS) consist of generating the $2N$ signals of the X vector using only one precalculated sine table, which is read sequentially by means of a time division multiplexing scheme to obtain the N considered harmonics within a base period (T_0). The implementation diagram of the proposed VF-DDS for N harmonics generation is presented in Fig. 1(a).

The VF-DDS generates the harmonic reference signals of sinus and cosine for the number of harmonics defined by N, using just one ROM memory with depth equal to 2^{P}. All harmonic signals $(2N)$ are generated and sent sequentially using a time-division multiplexing structure. The multiplexing process

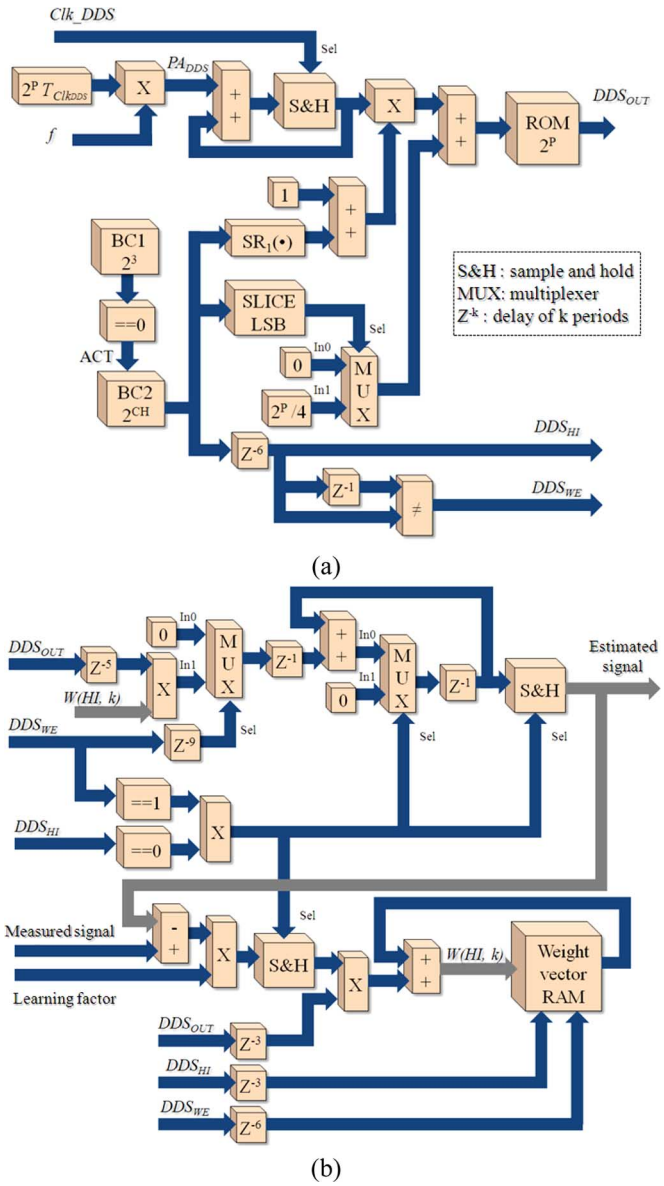


Fig. 1. Simplified diagram of (a) VF-DDS and (b) weight vector updating function ($\mathrm{WVU-T_0}$), where T_0 is the updating period.

is coordinated by two free-running counters BC1 and BC2. BC1 is a 3-b counter which generates the period necessary to produce the address and to access the ROM memory to obtain the information of each harmonic. BC2 is a CH-bits counter which is employed to generate the address information corresponding to each harmonic signal (sine and cosine). Since CH is defined as $\mathrm{ceil}\{\log_2(2N)\}$, then the output of BC2 varies from 0 to $2N-1$. Additional logic is employed to produce the proper addressing of the ROM memory for the sine and cosine signals generation. A SLICE LSB block is used to extract the LSB bit of its input which is related to the phase for the sine or cosine signal (0 for sine and $2^{\mathrm{P}}/4$ for cosine), and an $\mathrm{SR_1}$ (shift right one bit) block is used to obtain the harmonic order.

B. Weight Vector Updating (WVU)

Normally, the signal sampling period (T_S) and the DDS base period (T_0) are different depending on the characteristics of the

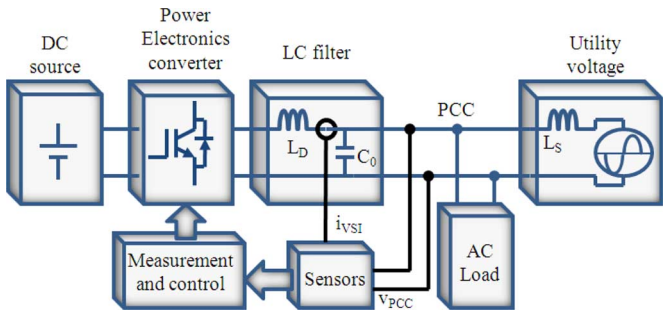


Fig. 2. Simplified circuit of grid-connected VSI.

analog-to-digital converter (ADC) employed in the measurement system, then the weight vector can be updated by means of two different WVU schemes as proposed in [19], using T_S or T_0 as the updating period. It has been demonstrated in [19] and [20] that the more efficient structure for FPGA implementation concerning the used area is the $\mathrm{WVU-T_0}$, which employs the DDS base period as updating period. In this case, the updating function including the learning rule and the signal estimation are implemented according to Fig. 1(b).

IV. Proposed Implementation of VSI Control

A simplified circuit of a grid-connected VSI system, as used for validation, is presented in Fig. 2, where $\mathrm{L_S}$ is the grid inductance, $\mathrm{L_D}$ and $\mathrm{C_0}$ are respectively the inductor and capacitor of the *LC* output filter of the VSI, and PCC is the point of common coupling.

The Fourier decomposition of the load voltage (v_{PCC}) and the output current of the VSI (i_{VSI}) can be obtained by using the ADALINE implementation presented in the previous section. These time-domain representations of voltage and current can be expressed according to

$$v_{\mathrm{PCC}}(t) = V_{\mathrm{PCC0}} + \sqrt{2}\sum_{n=1}^{\infty}\left[V_{\mathrm{PCC}\,An}\cos(n\omega t) + V_{\mathrm{PCC}\,Bn}\sin(n\omega t)\right] \quad [\mathrm{V}] \tag{4}$$

$$i_{\mathrm{VSI}}(t) = I_{\mathrm{VSI0}} + \sqrt{2}\sum_{n=1}^{\infty}\left[I_{\mathrm{VSI}\,An}\cos(n\omega t) + I_{\mathrm{VSI}\,Bn}\sin(n\omega t)\right] \quad [\mathrm{A}]. \tag{5}$$

The estimated fundamental voltage at the k instant can be obtained from the ADALINE using

$$v_{\mathrm{PCC1}}(k) = X(0,k)\cdot W(0,k) + X(1,k)\cdot W(1,k) \quad [\mathrm{V}] \tag{6}$$

and its amplitude can be computed using

$$|v_{\mathrm{PCC1}}| = \sqrt{W(0,k)^2 + W(1,k)^2} \quad [\mathrm{V}]. \tag{7}$$

Taking into account the estimated fundamental of $\mathrm{v_{PCC}}$ as the reference signal for the power control system, the orthogonal

reference signals for synchronization of the VSI are obtained using

$$\mathrm{REF}_{\sin}(k) = \frac{X(1,k)\cdot W(1,k) + X(0,k)\cdot W(0,k)}{\sqrt{W(0,k)^2 + W(1,k)^2}} \quad (8)$$

$$\mathrm{REF}_{\cos}(k) = \frac{X(1,k)\cdot W(0,k) - X(0,k)\cdot W(1,k)}{\sqrt{W(0,k)^2 + W(1,k)^2}}. \quad (9)$$

This approximation is only possible if the harmonics and the dc components of voltage at the point of common coupling are negligible. The DG interfaces, as recommended by IEEE standards [32], must be operated with low total harmonic distortion (THD). Under this restriction, the fundamental instantaneous power can be written using

$$p(k) = V_{\mathrm{PCC}}(k)\cdot I_{\mathrm{VSI\ B1}}\sqrt{2}\mathrm{REF}_{\sin}(k) + V_{\mathrm{PCC}}(k)\cdot I_{\mathrm{VSI\ A1}}\sqrt{2}\mathrm{REF}_{\cos}(k) \quad [\mathrm{VA}] \quad (10)$$

and the fundamental active and reactive powers ($\mathrm{p_1}$ and $\mathrm{q_1}$) can be computed using

$$p_1 = \frac{1}{\sqrt{2}}\left|v_{\mathrm{PCC1}}\right|\cdot I_{\mathrm{VSI\ B1}} \quad [\mathrm{W}]$$

$$-q_1 = \frac{1}{\sqrt{2}}\left|v_{\mathrm{PCC1}}\right|\cdot I_{\mathrm{VSI\ A1}} \quad [\mathrm{VAR}]. \quad (11)$$

The fundamental output current of VSI (i_{VSI1ref}) can be written as a function of v_{PCC} and the active and reactive power set points ($p_{1\mathrm{ref}}$ and $q_{1\mathrm{ref}}$) using

$$i_{\mathrm{VSI1\ ref}}(k) = \frac{2p_{1\ \mathrm{ref}}}{\left|v_{\mathrm{PCC1}}\right|}\mathrm{REF}_{\sin}(k) + \left(\frac{-2q_{1\mathrm{ref}}}{\left|v_{\mathrm{PCC1}}\right|} + \omega C_0\left|v_{\mathrm{PCC1}}\right|\right)\mathrm{REF}_{\cos}(k) \quad [\mathrm{A}]. \quad (12)$$

This expression is used to generate the reference current for the VSI current control. It also includes the current which corresponds to the reactive power of the filter capacitor (C_0). A hysteresis current control (HCC) modulator is employed to produce the gating pulses for the power electronics converter. The two different schemes of the ADALINE synchronization have been implemented and evaluated in this paper: ADALINE with FF-DDS and ADALINE with VF-DDS using a feedback loop with the mean frequency of the generated in-phase reference signal ($\mathrm{REF}\sin(k)$).

V. Implementation and Cost Evaluation of the Proposed ADALINE and Power Control Schemes

The proposed structures have been implemented for a single-phase VSI with a two-channel scheme (voltage and current measurements) by using Xilinx—System Generator and ISE Foundation for the Xilinx xc2vp30-7ff896 FPGA target [33], [34]. The implementation cost or device utilization after placing and routing of the proposed schemes (FF and VF-ADALINE) has been evaluated for different harmonic orders using T_0 as the weight updating period. According to the results for 4, 8, 16, 32, and 50 harmonics detection using the $\mathrm{WVU} - \mathrm{T_0}$ scheme, the slices utilization is always under 35% (4 920 slices for $\mathrm{N} = 50$) of the maximum available in the FPGA device (13 696) [33], [34]. The used slices, when increasing N from 4 to 50, are increased from 4365 to 4920 slices, which means by 12.7%.

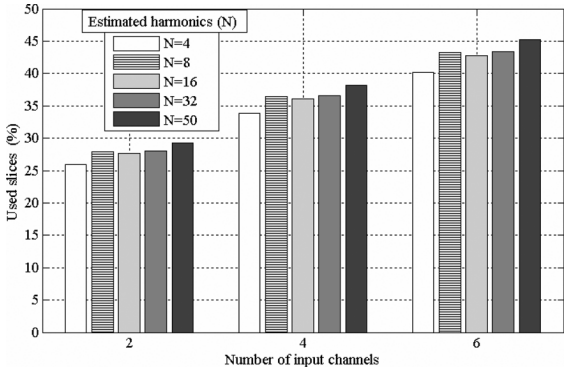


Fig. 3. Used slices in Xilinx xc2vp30-7ff896 target according the number of channels and the harmonic order. The available slices is 13696.

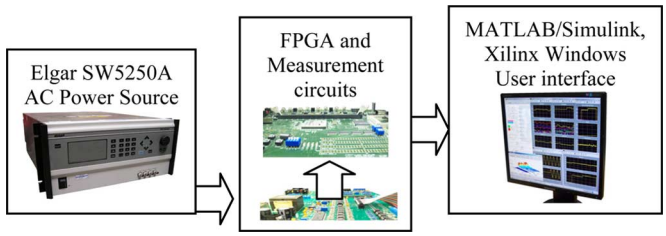


Fig. 4. Simplified structure of test bench used for the validation of voltage estimation and reference signals generation.

In order to verify the applicability of the proposed hardware implementation for multiphase systems, the device utilization for the implementation of the sampling and input buffers, the DDS, the $\mathrm{WVU}-\mathrm{T_0}$ and the fundamental signal restoring functions for different number of input channels and different harmonic order has been evaluated. As a result, for $\mathrm{N} = 32$, the slices utilization for the six-channels ADALINE is increased by 54.7% (5933) compared with the two-inputs ADALINE one (3835), and only 43% (5933/13696) of available resources in the FPGA are used. This means that, even if the number of channels is increased three times, the free FPGA area is superior to 50%, then the remaining resources could be used for the implementation of control and other complementary functions in single-phase or multiphase systems. Those results are gathered and presented in Fig. 3.

VI. Experimental Results

A. Voltage Estimation and Reference Signals Generation

The voltage estimation and the reference signals generation have been evaluated experimentally using a programmable ac source to generate a 120-V voltage signal with variable frequency. The frequency of the test signal is varied within the IEEE recommended limits [32] (within 59.3 and 60.5 Hz). The variations have been introduced in steps of 0.1 Hz. The two proposed synchronization methods have been implemented in parallel in the same FPGA. The structure of the test bench used for frequency tracking is presented in Fig. 4.

The trajectories of the measured voltage (sampled with 10-μ s period), the generated in-phase reference signal, and the frequency of the generated synchronization signal have been plotted

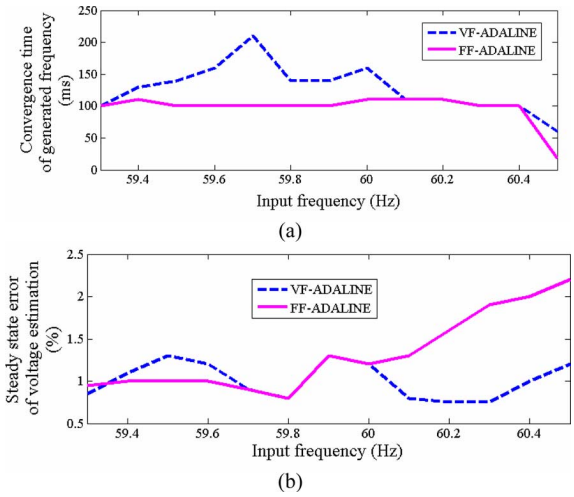


Fig. 5. Convergence time of (a) generated frequency and (b) steady-state error of voltage estimation using the proposed methods when the utility voltage is 120 V, frequency variations 59.3 to 60.5 Hz (0.1-Hz step), and $\mathrm{THD} = 1.5\%$.

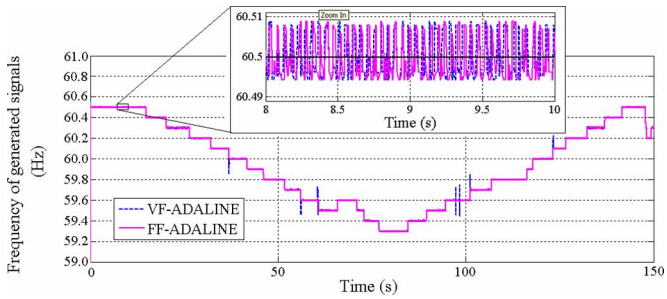


Fig. 6. Frequency tracking with the proposed methods.

by using the MATLAB/Simulink-Xilinx user interface to compare the performance of each method. The convergence of the frequency of the generated signals and the steady-state error of the voltage estimation have been plotted in Fig. 5 using the information of the measured voltage, the estimated voltage, the generated synchronization signals, and the computed frequency of generated synchronization signals. Also, the experimental results of frequency tracking are presented in Fig. 6.

Experimental results of Figs. 5 and 6 show that FF-ADALINE offers the best steady-state estimation error for frequencies below its reference frequency ($\mathrm{f} < 60$ Hz), and the worst one for frequencies above its reference frequency. VF-ADALINE offers good steady-state estimation error. The convergence time of frequency tracking is longer than the one obtained with FF-ADALINE. The frequency tracking error remains under ± 0.01 Hz in both schemes (inset of Fig. 6), so any of them can be used for synchronization with good transient response and accurate estimation, even for sudden frequency variations.

Additional experimental results show that FF or VF schemes can be used for synchronization with the following limitations: estimation error with FF-ADALINE increases over 3% when the frequency deviation is superior to ± 2 Hz; the learning factor of VF-ADALINE must be set below to 0.3 in order to keep stable orthogonal signals generation. A learning factor higher than 0.3 improves the convergence time, but it may also introduce undesirable overshoot in the frequency estimation and distortion in

TABLE I
FF-ADALINE PERFORMANCE UNDER DIFFERENT THD

	THD of test signal				
	1.5%	2%	3%	4%	5%
Convergence time (ms)	110	115	108	114	112
Steady state estimation error (%)	1.3	1.35	1.27	1.31	1.33

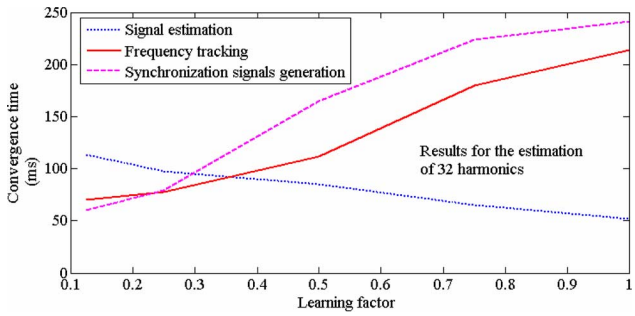


Fig. 7. Convergence time for different learning factors. Transient of amplitude (from 115 to 118 V), frequency (from 60.4 to 59.4 Hz) and phase angle (from 30° to 45°). FF-ADALINE scheme with $\mathrm{N} = 32$.

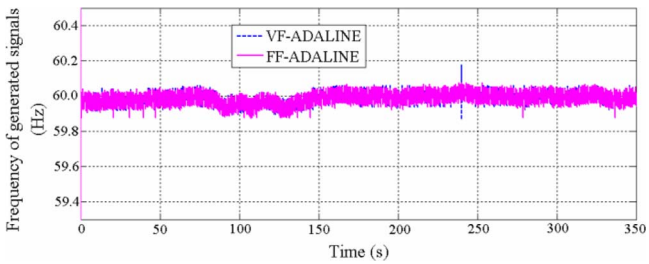
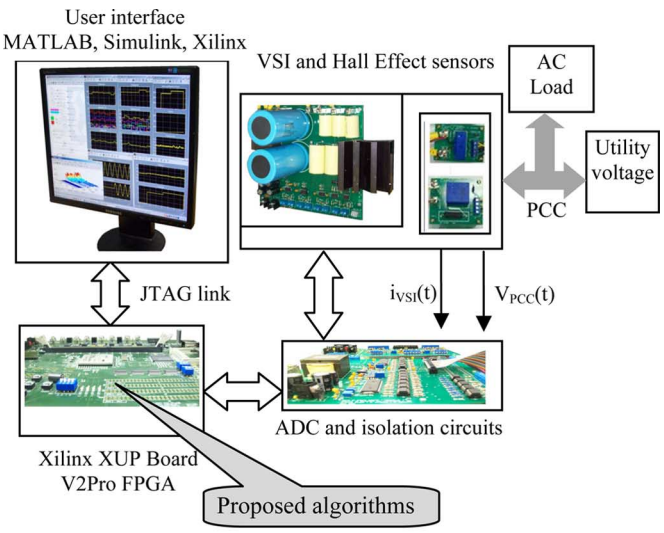


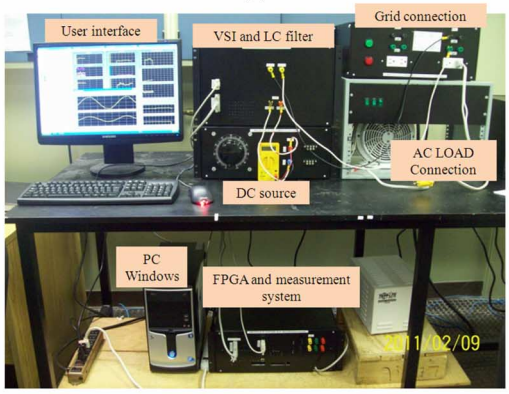
Fig. 8. Experimental results of the tracking of utility frequency with the two proposed methods.

the synchronization signals when important transients in measured signal are observed. Taking into account that it is expected that the THD of the measured signals could produce more important effects on the performance of estimation when using the FF-ADALINE scheme, it has been then evaluated under different voltage THD (from 1.5% to 5%) without important effects on the frequency tracking and the voltage estimation as reported in Table I. According to these results, the estimation error remains under 2% and the convergence time of generated signals under 120 ms.

The convergence time of the signal estimation, the frequency tracking, and the synchronization signals generation using FF-ADALINE with $\mathrm{N} = 32$ have been also evaluated considering a transient of frequency, phase, and amplitude. The results for different learning factors have been plotted in Fig. 7. According to these results, the synchronization signals generation and the frequency tracking can be improved by using a low learning factor. The convergence time of the frequency tracking is comparable or better than the one of the classic PLL and the MSOGI-FLL proposed in [11], even if high-order harmonics estimation is considered here. A low-order harmonic implementation offers a better convergence time. The experimental results of frequency tracking of the utility voltage during 350 s are presented in Fig. 8.



(a)



(b)

Fig. 9. (a) Functional diagram and (b) real view of test bench used for power control and power analysis of grid-connected VSI.

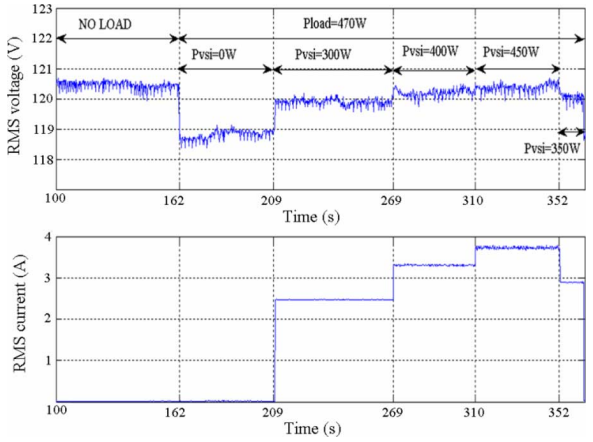


Fig. 10. Estimated rms values of $V_{\rm PCC}$ and $I_{\rm VSI}$ when signal estimation, synchronization, and power control of VSI uses FF-ADALINE scheme with $\rm F_{REF}$ = 60 Hz.

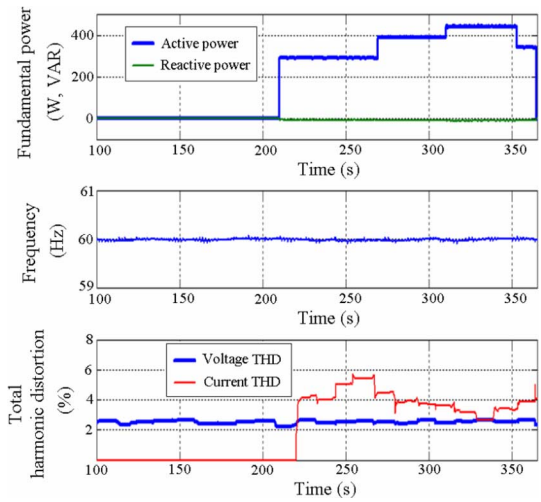


Fig. 11. Estimated VSI powers, frequency of generated signals and THD of $V_{\rm PCC}$ and $I_{\rm VSI}$ when signal estimation, synchronization, and power control of VSI use FF-ADALINE scheme with $\rm F_{REF}$ = 60 Hz.

These results confirm that the two methods offer good frequency tracking in this more realistic evaluation considering the utility voltage variations in frequency, in amplitude, and in harmonic content. The estimated mean frequency of the utility is within 60±0.1 Hz. This is well within the range of the Hydro-Québec frequency target values for normal conditions without disturbances that are established among 60±0.6 Hz [35]. According to the Hydro-Québec statistics, in normal conditions, frequency is within 60±0.2 Hz, in frequent disturbed conditions, frequency may be within 60±0.5 Hz and in rare disturbed conditions frequency may be within 60±1 Hz.

B. Power Control of Grid-Connected VSI

A functional diagram and a real view of the proposed and developed test bench used to validate the power control algorithms are presented in Fig. 9. Hall-effect sensors (LEM LV-25 and LAH-50P) are used to measure the $v_{\rm PCC}(t)$ and $i_{\rm VSI}(t)$ signals which are digitized with a 12-b ADC (AD1674) using a 10-μs sampling period. The digitized signals $v_{\rm PCC}(k)$ and $i_{\rm VSI}(k)$ are sent to the FPGA circuit as the input of the two-channels ADALINE to be used in the synchronization and control algorithms. VSI characteristics are presented in the Appendix.

The user interface is configured to generate the set point of VSI control ($p_{1\rm ref}$ and $q_{1\rm ref}$), and to visualize the real-time information of rms values of voltage and current, the estimated active and reactive powers, the measured frequency of the generated signals, the THD of voltage and current, the waveforms of the measured voltage and current, and the estimated spectrum of voltage and current ($V_{\rm PCC}$ and $I_{\rm VSI}$). In the two evaluated cases (FF-ADALINE and VF-ADALINE), the power setup of load and VSI presented in Table II has been employed.

The experimental results for the VSI synchornization and control using FF-ADALINE scheme are plotted in Figs. 10–12. Fig. 10 shows the trajectories of rms values of $V_{\rm PCC}$ and $i_{\rm VSI}$, for the different conditions of VSI output power. Notice that the measured voltage remains close to 120 V before the load is connected (no-load voltage). At load connection the voltage falls to its minimum (t = 162 s), and it rises with the increase of VSI output power (t = 209 s). As expected, when the VSI output power is close to the load power the voltage becomes also close to the no-load voltage.

Fig. 11 shows the estimation of active and reactive powers, the frequency of synchronization signals, and the THD of the $V_{\rm PCC}$ and $i_{\rm VSI}$. According to these results, the estimated active

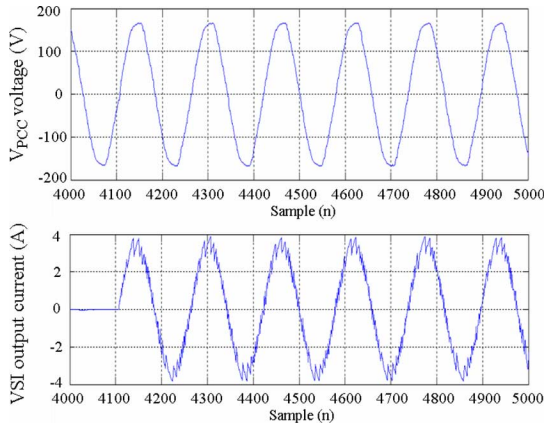


Fig. 12. $V_{\rm PCC}$ and $I_{\rm VSI}$ waveforms when signal estimation, synchronization and power control of VSI uses FF-ADALINE scheme with $F_{\rm REF} = 60$ Hz.

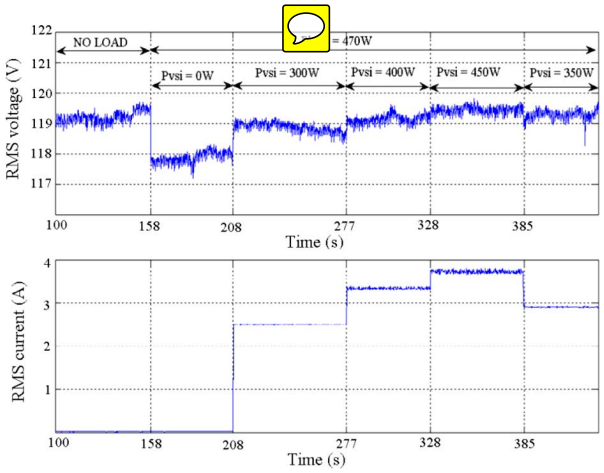


Fig. 13. Estimated rms values of $V_{\rm PCC}$ and $I_{\rm VSI}$ when signal estimation, synchronization, and power control of VSI uses VF-ADALINE scheme.

power of VSI corresponds to the set points, the frequency of the generated signals remains close to the frequency of the utility voltage (60 Hz), the THD of the voltage remains quite constant at between 2% and 3%, the THD of the current varies with the output power of VSI, and the minimum THD current is obtained when the output power of VSI is close to the load power. Fig. 12 shows the voltage and current trajectories at the start of VSI operation with active power set point $p_{1\rm ref} = 300$ W. The current wave has an important distortion because the hysteresis band of the current control is intentionally set to $\pm$ 350mA, and the output power of the VSI is low.

The experimental results for the VSI synchronization and control using VF-ADALINE scheme are plotted in Figs. 13–15. The trajectories of rms values of $V_{\rm PCC}$ and $i_{\rm VSI}$ (as in Fig. 10 for FF-ADALINE), for the different conditions of VSI output power are shown in Fig. 13.

Similar results are obtained concerning the voltage variations in relation with the output power of VSI and the load power. Fig. 14 shows the estimation of active and reactive powers, the frequency of the synchronization signals, and the THD of the $V_{\rm PCC}$ and $i_{\rm VSI}$ for the conditions of power already presented in Table II. Fig. 15 shows the voltage and current trajectories at the start of VSI operation with active power set point $p_{1\rm ref} =$ 300 W.

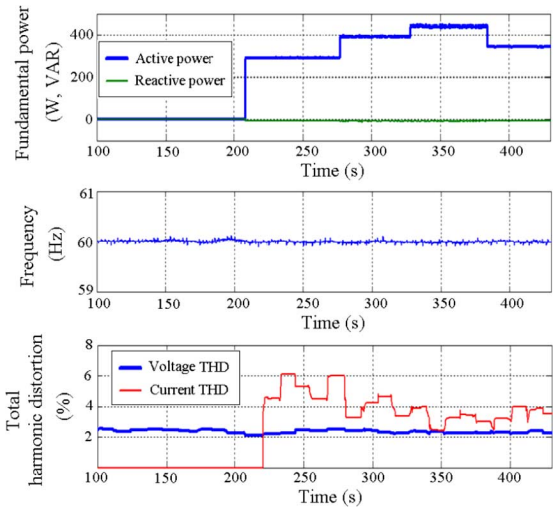


Fig. 14. Estimated VSI powers, frequency, and THD of $V_{\rm PCC}$ and $I_{\rm VSI}$ when signal estimation, synchronization, and power control of VSI use VF-ADALINE scheme.

TABLE II
POWER SETUP OF LOAD AND VSI

Setup	1	2	3	4	5	6	7
$P_{\rm LOAD}$ (W)	0	470	470	470	470	470	470
$P_{\rm 1REF}$ (W)	0	0	300	400	450	350	0

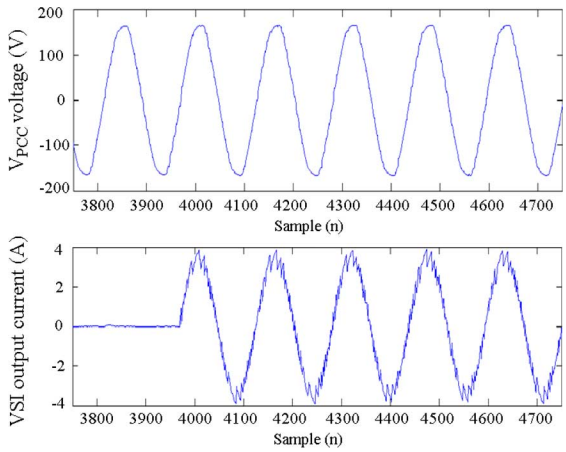


Fig. 15. $V_{\rm PCC}$ and $I_{\rm VSI}$ waveforms when signal estimation, synchronization, and power control of VSI uses VF-ADALINE scheme.

The results obtained by using the FF-ADALINE or VF-ADALINE methods for power control are similar; however, more stability is observed in the voltage and frequency tracking when FF-ADALINE is employed, mainly because the frequency of the utility voltage remains close to the nominal frequency. On the other hand, if FF-ADALINE is employed and the frequency of the utility voltage is not close to its nominal value, then the estimation error increases, in that case it would be more advantageous to use VF-ADALINE.

C. Harmonics Analysis

The estimation of harmonics and the transient response of the two proposed implementations of ADALINE (FF and VF) have been compared with the ones obtained by using

TABLE III
TIMING CONFIGURATION OF TEST SIGNAL (13)

	Time interval				
	0-0.3s	0.3-0.6s	0.6-0.9s	0.9-1.2s	1.2-1.5s
V	120	120	115	118	123
f	60	60.4	60.4	59.45	60
θ	45	45	45	30	30

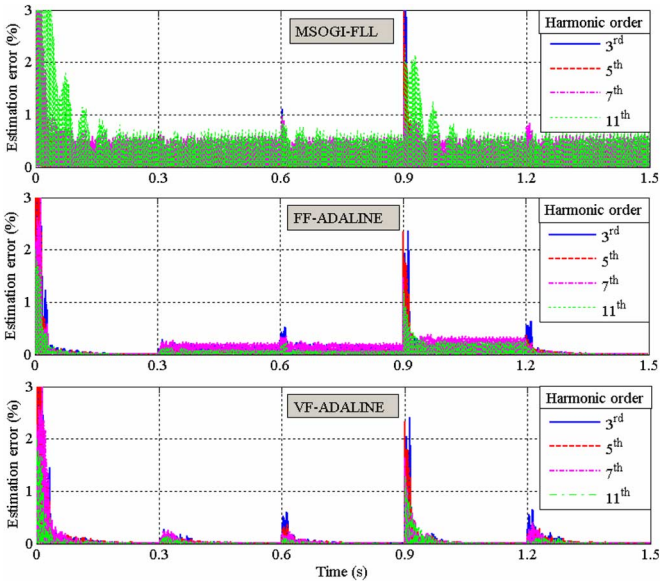


Fig. 16. Harmonics estimation error by using MSOGI-FLL, FF-ADALINE, and VF-ADALINE.

the MSOGI-FLL [11]. These three structures have been implemented in the same FPGA device and evaluated by using hardware in the loop co-simulation.

The test signal is defined by

$$v(t) = V\sin(2\pi ft+\theta) + 0.009V\sin(6\pi ft+\theta) + 0.017V\sin(10\pi ft+\theta) + 0.016V\sin(14\pi ft+\theta) + 0.0064V\sin(22\pi ft+\theta) + 0.0028V\sin(26\pi ft+\theta) \quad (13)$$

taking into account in Table III the timing configuration in order to consider voltage, frequency and phase variations. The results of the estimation error of the 3rd, 5th, 7th and 11th harmonics are plotted in Fig. 16. In terms of accuracy, it is to be noticed that the proposed methods (FF and VF-ADALINE) show better performance than MSOGI-FLL. This accuracy is going to be reflected in the power quality evaluation, in the orthogonal signals generation and consequently in the power control.

Figs. 17 and 18 present the time evolution of the estimated amplitude of the harmonics of the v_{PCC} and i_{VSI} signals, from the second to the 32nd harmonic by using FF-ADALINE and VF-ADALINE, respectively. Similar results are observed concerning the distribution of the estimated voltage harmonics, namely that, in both cases, they remain quite constant, and they are important mainly for the low-order harmonics (third, fifth, seventh, 11th, and 13th). The values of this harmonic distribution, as expected, are within the target values of Hydro-Québec for the medium and low level distribution voltages [36].

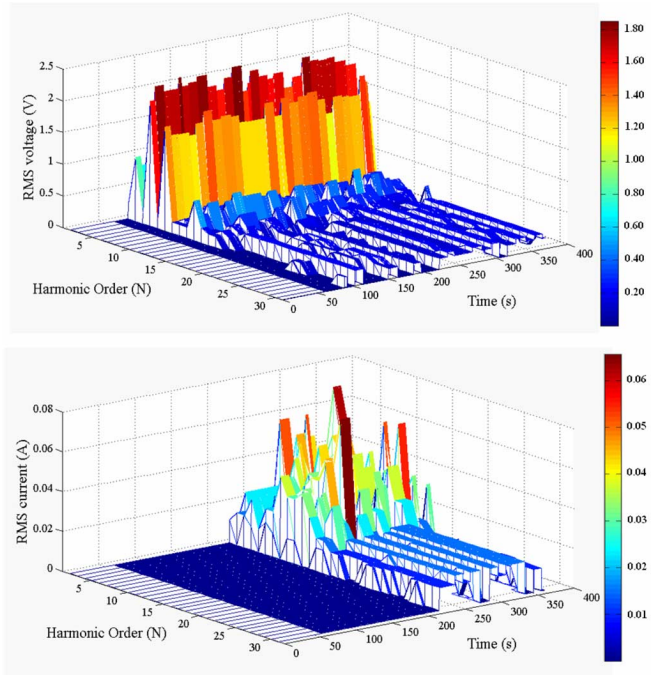


Fig. 17. Time evolution of estimated V_{PCC} and I_{VSI} spectrums when signal estimation, synchronization, and power control of VSI uses FF-ADALINE scheme with $\mathrm{F_{REF}} = 60$ Hz. $(2 < \mathrm{N} < 32)$.

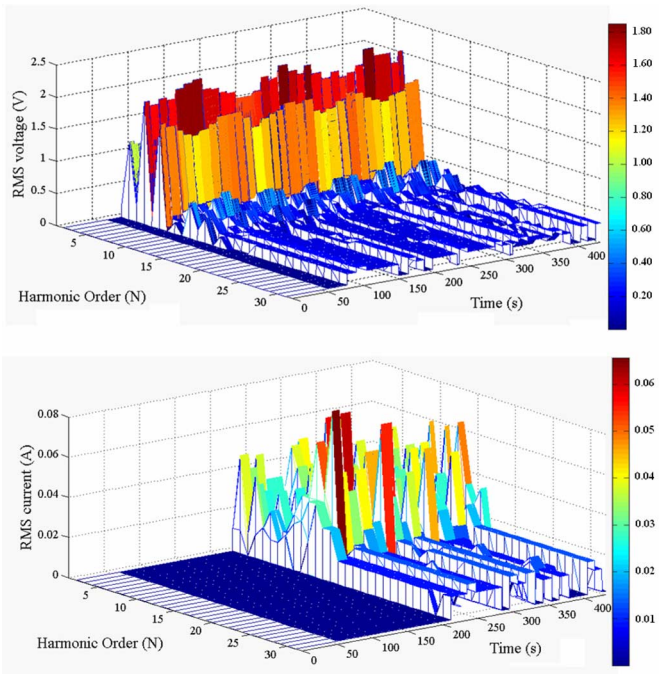


Fig. 18. Time evolution of estimated V_{PCC} and I_{VSI} spectrums when signal estimation, synchronization, and power control of VSI uses VF-ADALINE scheme. $(2 < \mathrm{N} < 32)$.

The distribution of harmonics of the estimated VSI output current in both cases is variable and more widely dispersed from the second to the 20th harmonic. Low-order harmonics are expected to appear when a large hysteresis band is employed, as in this case (±350 mA). One can also expect to reduce or to eliminate some components of the harmonics by reducing the

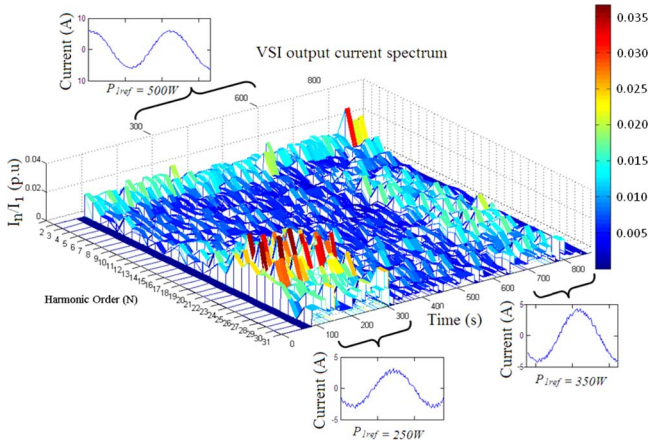


Fig. 19. Time evolution of the estimated VSI output current spectrum, using FF-ADALINE ($\mathrm{N} = 32$ and $\mathrm{WVU}-\mathrm{T}_0$) according to the output power of VSI.

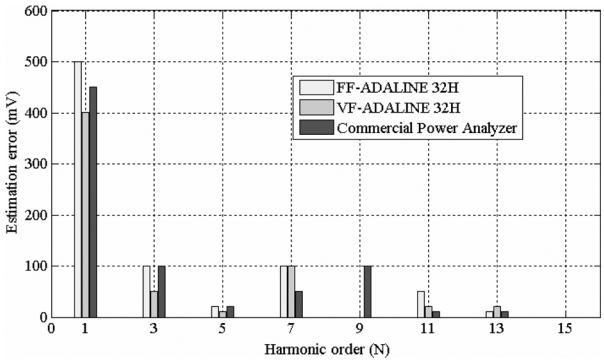


Fig. 20. Error of V_{PCC} estimation using FF-ADALINE, VF-ADALINE, and commercial power analyzer compared with FFT computed by MATLAB. Only the most significant voltage harmonics are plotted. Nominal utility voltage is 120 V/60 Hz. Full scale of measurement systems is $\pm$250 V.

hysteresis band or by using advanced pulsewidth modulation (PWM) techniques.

The online power quality analysis including the tracking of voltage and current spectrums, as proposed in this paper, is very useful for the evaluation of power electronics converters to verify if they meet the power quality standards for grid-connected operation [32] and the particular requirements of the local utility operator. Fig. 19 shows, as an example, the time evolution of the normalized current spectrum of VSI according to the variations of the output power.

The mean values within one second of the estimated harmonics amplitude of the measured voltage have been computed and compared with the ones obtained by means of commercial power analyzer HIOKI 3196. The harmonics of the measured signals have been also computed offline by means of the FFT function available in MATLAB software.

The results of the estimation error considering the FFT values as the reference have been plotted in Fig. 20. Even if similar results are obtained by the three methods, VF-ADALINE offers the best harmonics estimation with the lowest error. A better performance could be obtained by improving the ADCs resolution (in this case, 12 b).

TABLE IV
SUMMARY OF RECENT LITERATURE METHODS

Method/ plateform/ year/ [ref]	N	T_C (µs)	T_S (µs)	Function
Multi-resonant Frequency-locked Loop MSOGI-FLL/ DSP/ 2011/ [11]	7 selected harmonics	26	100	HD, FD, OSG
Radial Basis Function Neural Network/Personal Computer/ 2010 / [10]	8 selected harmonics	123	1/(64*f*)	HD
Algorithm based on DFT/ DSP-FPGA / 2009/ [12]	3 selected harmonics	N.A	125	HD, FD
Hardware implementation of ADALINE proposed in this work	Up to 50	8 (for N=50)	10	HD, FD, OSG

N: analyzed harmonics, T_C: computational time, T_S: signal sampling period, N.A. not available, HD: harmonics detection, FD: frequency detection, OSG: orthogonal signals generation.

D. Comparison With Some Recent Literature Works

A comparison of the proposition with some recent literature works of harmonics detection with applications in power systems and with experimental validation [10]–[12] is summarized in Table IV. Here, the proposed hardware implementation of ADALINE shows important advantages concerning the short computational and sample times, the high number of analyzed harmonics, and the implemented functions. The implementations with selected harmonics normally reported in literature show complexities and computational times that make possible their utilization in real-time applications. However, the performance of that kind of implementation can be affected when not selected harmonics are present in the measured signal.

The proposed hardware implementation allows the estimation of a high number of harmonics with a very low execution time, in fact for $\mathrm{N} = 50$ and a 10-ns FPGA clock period, the maximum sampling rate of measured signals is 125 kS/s. The experimental sampling rate is 100 kS/s which is imposed by the characteristics of the used ADC circuit. It is important to remark that all information is updated and available for transmission within the sampling period, and then the real-time performance is not limited by the algorithm but by the data channel bandwidth. In the implemented test bench, a USB link at 12 Mbps has been employed to send the full information (real-time clock information, harmonics, frequency, and power) of the two measured channels to the user interface using a 10-ms sampling period. Current and voltage waves are also sent to the user interface by using a first-in first-out (FIFO) buffer.

VII. CONCLUSION

This paper presents a comparative evaluation of two real-time power control and analysis schemes based on hardware implementation of ADALINE for FPGA. The proposed structures allow the generation of the orthogonal signals which have been successfully used for the synchronization of a grid-connected VSI and the real-time analysis of the power quality.

The first method works at a fixed frequency and the second one offers the possibility of variable-frequency harmonics estimation being more accurate in signal estimation even if the frequency of the utility voltage is not at its nominal value. Both

methods have been evaluated by experimentation with satisfactory results for both signal estimation and power control of the grid-connected VSI.

The proposed innovative and efficient hardware implementations show many advantages in contrast to software or co-design solutions, allowing the implementation in only one programming device and reducing the system complexity and the processing time. Additionally, with the proposed approaches, the saved area can be used for the embedded implementation of multiple algorithms in the same device without increasing the processing time.

These advantageous characteristics of the proposition are ideal for use in future SIMs, which could be used not only for power dispatch from DER to the utility grid but also for the compensation of harmonics and reactive power, the monitoring of power quality, and other complementary functions.

APPENDIX

A. Experimental Setup Parameters

- AC power source: 120 VAC/60 Hz.
- Signals sampling period: $\mathrm{T_s} = 10\ \mu$s.
- Number of estimated harmonics: $\mathrm{N} \leq 50$ (limited by FPGA clock period).
- Learning factor: $0.125 \leq \alpha \leq 1.0$
- FPGA clock period: $\mathrm{T_{FPGA}} = 10$ ns.
- ROM sine table length/resolution: $2^{\mathrm{P}} = 2^{15}/18$ b.
- Multipliers input/output resolution: 18 b/35 b.

B. Power Electronics Converter Characteristics

- Voltage source inverter.
- 16 A, 600 V IGBT full bridge (IRAMX16UP60A).
- Output filter $\mathrm{L_D} = 17$ mH, $\mathrm{C_0} = 1\ \mu$F.
- DC source voltage: 195 V.

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Alben Cardenas (S'09–M'12) received the B.S. degree in electronic engineering from the Antonio Nariño University, Villavicencio, Colombia, in 2003, and the M.S. degree in electrical engineering from the Université du Québec à Trois-Rivières (UQTR), Trois-Rivières, QC, Canada, in 2008, where he is currently working toward the Ph.D. degree in electrical engineering.

He is currently a Researcher with the Hydrogen Research Institute (HRI), UQTR. His research interests include renewable energy, distributed generation, power electronics and embedded systems for energy conversion and power quality.

Mr. Cardenas is junior member of the Ordre des Ingénieurs du Québec and a member of the IEEE Power and Energy Society and the IEEE Industrial Electronics Society.

Cristina Guzman (S'10) received the B.S. degree in electrical engineering from the Université du Québec à Trois-Rivières (UQTR), Trois-Rivières, QC, Canada, in 2010, where she is currently working toward the M.S. degree in electrical engineering.

She is currently a Research Assistant with the Hydrogen Research Institute (HRI), UQTR. Her research interests include distributed generation, power electronics for energy conversion and power quality.

Mrs. Guzman is student member of the IEEE Power and Energy Society and the IEEE Industry Applications Society.

Kodjo Agbossou (M'98–SM'01) received the B.S., M.S., and Ph.D. degrees from the Université de Nancy I, France, in 1987, 1989, and 1992, respectively, all in electronic measurements.

He is now a head of the Engineering School, Université du Québec à Trois-Rivières (UQTR), Trois-Rivières, QC, Canada. He was a Post-Doctoral Researcher (1993–1994) with the Electrical Engineering Department, UQTR, and he was a Lecturer (1997–1998) with the same department. Since 1998, he has been an Associate Professor and, since 2004, a Full Professor with the Electrical and Computer Engineering Department of UQTR. He was the head of the department. He was also the Director of Graduate Studies in Electrical Engineering. His present research activities are in the area of renewable energy, integration of hydrogen production, storage and electrical energy generation system, control and measurements. He is a member of Hydrogen Research Institute and Research group "GREI" of UQTR. He is the author of more than 150 publications and holds four patents.

Prof. Agbossou is a member of the IEEE Power and Energy Society, the IEEE Industry Applications Society, the IEEE Communications Society, and the IEEE Industrial Electronics Society Technical Committee on Renewable Energy Systems. He is also a former Chair of the IEEE Section Saint Maurice, QC, Canada. He is a Professional Engineer and joined the Ordre des Ingénieurs du Québec in 1998.